REMARKS

Claims 1-23 are pending in the application. Claims 1 has been amended and claims 13-23 have been added by the foregoing amendment. Support for this amendment may be found, for example, in Figure 30 and in the description on pages 29 and 30.

§ 102 Rejections

Claims 1, 4-6, 8 and 12 stand rejected under 35 U.S.C. §102 (b) as allegedly being anticipated by U.S. Patent No. 6,064,679 ("Hashemi").

Claim 1 has been amended to emphasize the open-ended nature of a bus architecture according to exemplary embodiments. New independent claim 13 is directed to an integrated processing device, with the bus architecture features of claim 1. The comments made below in relation to claims 1 to 12 also apply to claims 13 to 23.

Hashemi describes an architecture designed to provide a hub port that internally synchronises signals passing around a *loop* network having characteristics similar to Fibre Channel Arbitrated Loop (FC-AL) networks. Hashemi achieves this by using a local clock signal within the hub port to control data transmission out of the hub port. The overall architecture consists of a plurality of hub ports (such as 102-112 in Figure 1A) connected in a *closed loop* by intermediate pipeline stage links (such as 114-124 in Figure 1A). Certain of the hub ports are connected to node ports (such as 126-132 in Figure 1A).

In the description of a hub port in Figure 3, Hashemi explains that incoming data from an upstream link 302 is encoded 306 and transmitted 308 to a node port 314 via a serialiser/deserialiser (SERDES) 310. The data is clocked at the incoming clock rate. When the node transmits data for transmission to a downstream hub port, the clock is extracted from the

data by the SERDES and that clock is used to control data transmission through receive circuit 318 and decoder 320 to a smoothing FIFO buffer 324. The data clock is also used to control sync detector 322, whose output is used in FIFO control 326 to control the FIFO buffer 324 and to instruct output control 328 to operate output multiplexer switch 334.

The output control 328 is responsible for switching the multiplexer 304 to one of three modes. In the first mode, the hub port is placed in bypass mode when there is no data originating from the node port, so that data incoming on input line 302 passes to the next downstream hub port.

In the second mode, when data is to be put onto the output line 338, the data is read out from the FIFO buffer 324 at the local clock rate by a local clock signal obtained over clock supply line 336. In this way, any variation in clock frequency/phase between the node port and the hub port is neutralized.

In the third mode, where word filling or deletion is to be affected, a fill word detector 330 instructs fill word generator 332 to add/remove words at appropriate intervals (i.e. between frames) and the multiplexer is switched to output the data from the fill word generator 332.

Hashemi differs from exemplary embodiments as recited in claim 1 in that, whereas Hashemi's architecture is based on a *loop* structure, claim 1 recites an open-ended path. More specifically, claim 1 recites, *inter alia*, *"a plurality of bus portions arranged in an open-ended series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit"*. There cannot be a "last in the series" in Hashemi as the architecture of Hashemi comprises a closed loop. Therefore, the assertion in the Office Action (¶3 of the Office Action) that Hashemi discloses "a plurality of bus portions arranged in series,

each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit", is simply incorrect.

The architecture described by Hashemi must use a loop structure because data packets in Hashemi can only travel in one direction. In contrast, in a bus according to exemplary embodiments, communication is bidirectional, so the bus can be open ended. Moreover, the bus architecture according to exemplary embodiments is an on-chip fixed topology bus, in contrast to Hashemi's flexible and re-wirable network bus. There are significant technical distinctions between these types of bus(es) that render the closed loop structure of Hashemi unsuitable for the purposes to which the Applicant's modular topology is applied.

As a further distinction on the basis of the on-chip nature of the Applicant's bus, the fibre channel in Hashemi uses a serial protocol (it has SERDES and clock recovery blocks), which may be appropriate for a network, but is inappropriate for an on-chip bus.

At least for these reasons, it is believed that claim 1 is not anticipated by Hashemi. Accordingly, claim 1 is allowable over the teachings of Hashemi. Claim 12 is similarly allowable over the teachings of Hashemi. Claims 2-11, all of which depend on claim 1 and recite additional advantages are also allowable.

With respect to claim 4 for example, the Office Action divides the single closed loop structure in Figure 1A of Hashemi into a "primary" bus 104 and a "secondary" bus 116, 118, 120, interconnected by an "interface" 104, which is actually one of the hub ports of Hashemi (equivalent to one of the bus-connection units of claim 1). This is an improper interpretation of the claims and of Hashemi's disclosure. However, this interpretation fails since claim 4 requires "a first *plurality* of modules connected to the primary bus". The single module 126 in Hashemi

does not constitute a "plurality". Therefore, Hashemi does not include all of the features recited in claim 4. Accordingly, claim 4 is allowable over the teachings of Hashemi.

It is also unreasonable (i.e. in the Office Action) to select an arbitrary bus segment of Hashemi as the primary bus in the loop. The primary-secondary bus architecture according to exemplary embodiments is asymmetrical, and the primary bus is shorter than the secondary bus. There may also be multiple secondary buses, which would not be possible in Hashemi's ring bus structure.

With respect to claim 5, the Office Action states that Hashemi discloses the arbitration feature of claim 5 (relying on column 1, lines 43-45 of Hashemi). However, this portion of Hashemi refers to one of three known ways of deploying conventional Fibre Channel networks and is not a disclosure within the context of the description of the network described by Hashemi. Hashemi does not disclose all of the features recited in claim 5 (such as the arbitration feature). Consequently, Hashemi fails to anticipate claim 5.

With respect to claim 6, the Office Action asserts that it is anticipated by Hashemi. Applicant's objection to this assertion is based on the same premise as highlighted above with respect to claim 4 (i.e. that the primary and secondary pipelined buses are formed by sub-division of the closed loop of Hashemi). Therefore, the rejection of claim is invalid for the same reason as that of claim 4. In addition, claim 6 is dependent from claim 5, which itself is also not anticipated by Hashemi as described above.

<u>§ 103 Rejections</u>

Claims 2 and 3 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Hashimi. Claim 7 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable

over Hashimi in view of U.S. Patent No. 6,057,863 ("Olarig"). Claim 9 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Hashimi in view of U.S. Patent No. 5,128,926 ("Perlman"). Claims 10 and 11 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Hashimi in view of U.S. Patent No. 5,925,118 ("Revilla").

The deficiencies of Hashemi with respect to claim 1, as highlighted above, are also applicable to claims 2 and 3. In particular, it is inconceivable that a person skilled in the art would consider Hashemi as a gateway to arriving at the presently claimed invention - one of ordinary skill in the art simply would not consider it a viable option to "cut" the closed loop of Hashemi and make it an open-ended series, as recited in claim 1 (from which claims 2 and 3 depend).

Similarly, with respect to claims 7 and 9 - 11, the deficiencies of Hashemi are not overcome by Olarig (claim 7), Perlman (claim 9) and Revilla (claims 11 and 11). Accordingly, claims 7 and 9-11 are all allowable over the cited art.

Claims 1, 5 and 12 stand rejected under 35 U.S.C. §102 (e) as allegedly being anticipated by U.S. Patent Nos. 6,055,228 ("DeKoning") and 5,548,733 ("Sarangdhar") even though the rejection appears to utilize an obviousness type analysis combining DeKoning and Sarangdhar.

DeKoning describes an FC-AL daisy-chained loop, in which a special connection unit permits interconnected loops to be reconfigured in the event of failure of a loop, which would otherwise prevent data transmission between devices connected to the loops (see abstract). The Office Action refers specifically to Column 1, lines 42-56 in connection with the feature that data traverses the bus architecture over a plurality of system clock cycles. However, this portion of DeKoning draws a distinction explicitly between daisy-chained configurations and bus

configurations. There are particular features of both (i.e daisy-chained configurations and bus configurations) that set them apart, as DeKoning outlines in the passage.

The Office Action asserts that it would be obvious to construct the DeKoning device with the pipelined bus of Sarangdhar. However, the teaching in DeKoning is very much to the effect that there is a dichotomy between daisy-chained and pipelined bus architectures. DeKoning teaches away from integrating features from the two configurations. It is, therefore, not the case that a person of ordinary skill in the art would import a feature disclosed in connection with the daisy-chained configuration taught by DeKoning into the totally different, technically distinct pipelined bus configuration. The fact that DeKoning is confined exclusively to a loop or a plurality of interconnected loops and fails to teach a serial, open-ended, bus architecture is not counteracted by attempting to shoe-horn into DeKoning a generic pipelined bus architecture as taught in Sarangdhar.

The combined teachings of DeKoning and Sarangdhar fail to disclose exemplary embodiments as recited in claim 1. At least for these reasons, it is believed that claim 1 is allowable over the DeKoning/Sarangdhar combination. Claim 12 is also allowable for similar reasons. Claim 5 which depends on claim 1, is also allowable over the DeKoning/Sarangdhar combination.

With respect to claim 5, the portions of DeKoning relied upon by the Office Action (i.e. at column 1, lines 57-67) merely describe the generic prior art as applied to pipelined buses in general. This passage does not constitute a statement that renders claim 5 obvious.

All of the rejections having been overcome, it is believed that this application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions with respect to expediting the prosecution of this application, she is urged to contact the undersigned at (703) 893-8500.

Respectfully submitted,
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Date: July 30, 2007